## CLAIMS

1. A structure comprising:

a substrate having a top surface and a bottom surface;

a first semiconductor die and a second semiconductor die attached to said top surface of said substrate;

a first heat spreader and a second heat spreader attached to said bottom surface of said substrate;

a first via and a second via in said substrate;

said first via providing a connection between said first semiconductor die and said first heat spreader, said second via providing a connection between said second semiconductor die and said second heat spreader.

2. The structure of claim 1 wherein said first and second heat spreaders are attached to a printed circuit board.

3. The structure of claim 1 further comprising a first substrate down bond area attached to said top surface of said substrate, wherein said first via provides an electrical connection between said first substrate down bond area and said first heat spreader.

4. The structure of claim 3 wherein a first semiconductor die ground bond pad on said first semiconductor die is electrically connected to said first substrate down bond area by a first down bonding wire.

5. The structure of claim 1 wherein a third via in said substrate provides a connection between a first signal bond pad of said first semiconductor die and a printed circuit board.

6. The structure of claim 1 wherein said substrate comprises organic material.

7. The structure of claim 6 wherein said organic material is selected from the group consisting of polytetrafluoroethylene material and an FR4 based laminate material.

8. The structure of claim 1 wherein said substrate comprises a ceramic material.

9. The structure of claim 5 wherein said third via provides an electrical connection between a first substrate bond pad and said printed circuit board, wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die.

10. The structure of claim 9 wherein said first substrate bond pad overlaps said third via.

11. The structure of claim 9 wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die by a first signal bonding wire.

12. The structure of claim 5 wherein said third via provides an electrical connection between said first signal bond pad of said first semiconductor die and a first land, said first land being electrically connected to said printed circuit board.

13. The structure of claim 12 wherein said third via overlaps said land.

14. A structure comprising:

a substrate having a top surface and a bottom surface;

a first semiconductor die and a second semiconductor die attached to said top surface of said substrate;

a heat spreader attached to said bottom surface of said substrate;

a first via and a second via in said substrate;

said first via providing a connection between said first semiconductor die and said heat spreader, said second via providing a connection between said second semiconductor die and said heat spreader.

15. The structure of claim 14 wherein said heat spreader is attached to a printed circuit board.

16. The structure of claim 14 further comprising a first substrate down bond area attached to said top surface of said substrate, wherein said first via provides an electrical connection between said first substrate down bond area and said heat spreader.

17. The structure of claim 16 wherein a first semiconductor die ground bond pad on said first semiconductor die is electrically connected to said first substrate down bond area by a first down bonding wire.

18. The structure of claim 14 wherein a third via in said substrate provides a connection between a first signal bond pad of said first semiconductor die and a printed circuit board.

19. The structure of claim 18 wherein said third via provides an electrical connection between a first substrate bond pad and said printed circuit board, wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die.

20. The structure of claim 19 wherein said first substrate bond pad overlaps said third via.

21. The structure of claim 19 wherein said first substrate bond pad is electrically connected to said first signal bond pad of said first semiconductor die by a first signal bonding wire.

22. The structure of claim 18 wherein said third via provides an electrical connection between said first signal bond pad of said first semiconductor die and a first land, said first land being electrically connected to said printed circuit board.

23. The structure of claim 22 wherein said third via overlaps said land.

24. A method for fabricating a structure for receiving first and second semiconductor dies, said method comprising steps of:

drilling first and second holes in a substrate;

filling said first and second holes with metal to form respectively first and second vias;

patterning first and second support pads on a top surface of said substrate, and patterning first and second heat spreaders on a bottom surface of said substrate;

said first via providing an electrical connection between said first heat spreader and said first support pad, said first support pad being suitable for receiving said first semiconductor die;

said second via providing an electrical connection between said second heat spreader and said second support pad, said second support pad being suitable for receiving said second semiconductor die.

25. The method of claim 24 further comprising the steps of:

drilling a third hole in said substrate;

filling said third hole with metal to form a third via;

patterning a first substrate bond pad on said top surface of said substrate, and patterning a first land on said bottom surface of said substrate, said third via providing an electrical connection between said first substrate bond pad and said first land.

26. The method of claim 24 further comprising a step of attaching said first and second semiconductor dies to respectively said first and second support pads.

27. The method of claim 24 further comprising a step of patterning a first substrate down bond area on said top surface of said substrate, said first substrate down bond area being electrically connected to said first support pad.

28. The method of claim 27 further comprising a step of electrically connecting a first ground bond pad of said first semiconductor die to said first substrate down bond area by a first down bonding wire.

29. The method of claim 25 further comprising a step of electrically connecting a first signal bond pad of said first semiconductor die to said first substrate bond pad by a first signal bonding wire, wherein said first signal bond pad of said first semiconductor die is electrically connected to said first land.

30. The method of claim 24 further comprising a step of soldering a printed circuit board to said first and second heat spreaders, wherein said printed circuit board is electrically connected to said first and second support pads.